M-3

WIDE-BAND LIMITING AMPLIFIERS WITH LOW SECOND HARMONIC DISTORTION, UTILIZING GaAs MMIC LIMITERS

E. J. Crescenzi Jr., R. S. Besser, B. A. Tucker, and T. R. Kritzer

Watkins-Johnson Company

Palo Alto, California

Abstract

A 2-6 GHz microwave limiting amplifier has been constructed using alternating MMIC limiters and GaAs FET amplifier stages. The function of the limiters is to restrict signal levels such that the gain stages operate in a linear region. A multistage prototype amplifier maintained second harmonic levels at least 28 dB below the fundamental output, when driven 30 dB into saturation.

Introduction

Instantaneous frequency measurement (IFM) receivers, channelized receivers, and frequency memory loops (FMLs) generally require high gain limiting amplifiers, often with bandwidths exceeding one octave. The normal operating dynamic range encountered in these applications can result in substantial gain compression; 30 to 50 dB of overdrive is not unusual. Driving an amplifier designed only for small signal operation with such high input levels frequently causes second harmonic generation equal to the fundamental output. Amplifiers specifically designed to perform a limiting function have been reported [1] which achieve -12 dBc typical second harmonic levels. An objective of this work has been to achieve -25 dBc maximum second harmonic levels over large signal dynamic ranges and wide bandwidths, through control of the specific limiting mechanism. The reduction of second harmonic content can result in improved IFM receiver dynamic range, and for FML applications, is expected to be strongly correlated with improvements in small signal suppression [2, 3].

Design Approach

The limiting amplifier architecture, shown in Figure 1, consists of alternating limiters and GaAs FET amplifier stages, cascaded such that the limiters restrict signal levels to a nominally linear range of operation for the amplifier stages. The role of the limiters is demonstrated in Figure 2, where various operating parameters are defined in the conventional manner.

The relative second harmonic level for a single amplifier stage driven heavily into saturation is:

$$R'_2 = P_{SAT} - P'_2$$

R'_2 is a complex function [2], particularly dependent on the dc operating point of the GaAs FETs and the output impedance matching circuitry. Wide-band amplifiers designed for optimum output power typically achieve R'_2 of 15 - 20 dB, although such levels can be difficult to maintain consistently in a manufacturing environment. For a limiter followed by an amplifier stage, where the limiter is saturated but the amplifier stage operates in a linear region:

$$R_2 = P_{I2} - G\,P_{OL}$$

The second harmonic contribution of the limiter is assumed to be much less than that of the amplifier stage. The relative second harmonic level (R_2) is thus a function of the limiter output power level (P_{OL}), amplifier gain (G), and amplifier intercept point (P_{I2}). A potential advantage of the limiter-amplifier approach is that R_2 is more readily predicted and more consistently controlled in a manufacturing environment than for a conventional limiterless design.

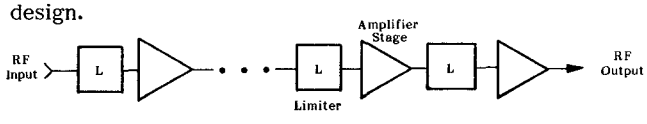

Figure 1. Limiting Amplifier Block Diagram

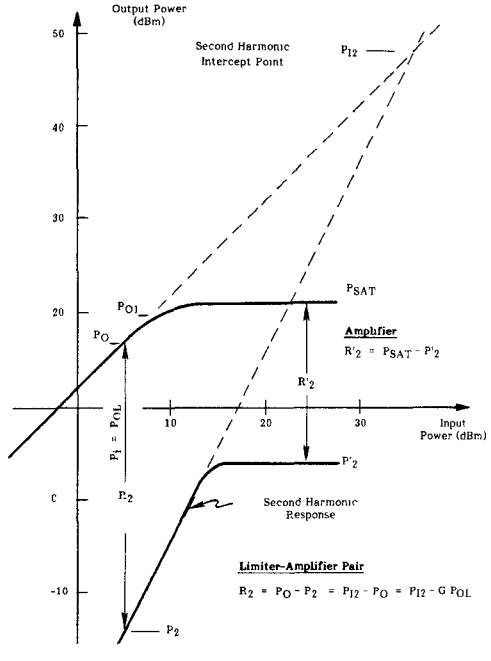

Figure 2. Second Harmonic Levels for an Amplifier and Limiter - Amplifier Pair

Limiter Design

The limiter, shown schematically in Figure 3, incorporates two anti-parallel shunt diode pairs at the input and output, separated by a series diode bridge. Limiting thres-

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hold is adjusted by changing the bias current through the series bridge, whereas output power at higher input levels is restricted by the shunt elements. This basic circuit was first realized [4] in 1975 using discrete silicon diodes and hybrid construction . A GaAs MMIC realization substantially extends the operating bandwidth by reducing parasitics associated with interconnection of the eight Schottky diodes and by optimizing bridge diode capacitance. The shunt-series bridge-shunt diode limiter offers the advantages of 1) adjustable threshold, 2) extended input dynamic range, and 3) absence of frequency sensitive distributed elements, relative to previously reported limiters [3].

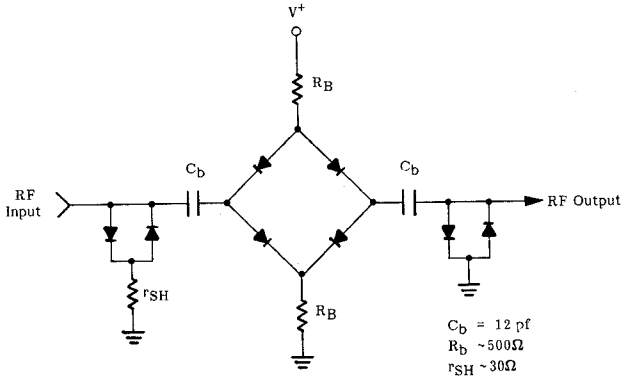

Figure 3. Shunt-Series Bridge-Shunt Schottky Diode Limiter

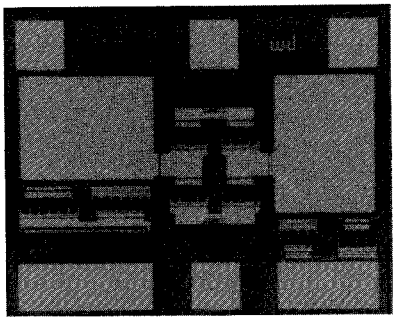

Figure 4. Monolithic GaAs IC Limiter (Die size is 575 µm by 475 µm)

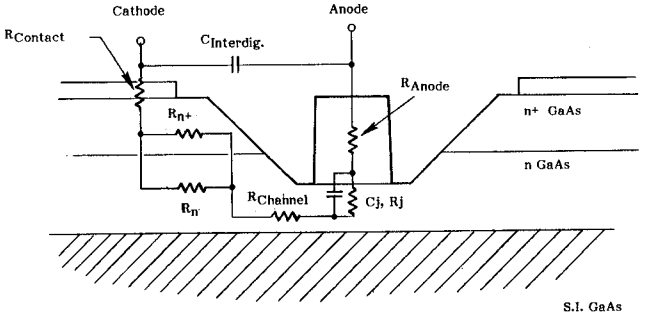

Figure 5. Limiter GaAs Schottky Diode Cross-Section

Monolithic Limiter Design and Fabrication

The limiter chip is shown in Figure 4. RF input and output connections are made at the upper left and right bonding pads respectively. The three lower pads provide grounding. Bridge bias is applied at the top central pad. The two large rectangular areas on the right and left halves of the chip are silicon nitride MIM capacitors. The eight interdigitated structures are the Schottky diodes. The bias resistors are visible adjacent to the dc pads. Immediately above the left ground pad lies the input resistor.

The Schottky diode device parameters form the principal consideration in selecting wafer starting material for the limiter IC process. Each diode can be modeled as a parasitic resistance in series with paralleled junction capacitance and resistance. Bridge diode series resistance contributes directly to insertion loss while the junction capacitance permits RF signal leak-through at higher frequencies.

The parasitic element values are controlled via the device geometry and doping levels. Anode dimensions were constrained by electromigration at high RF power levels. The active layer doping was chosen by optimization between the junction capacitance and the series resistance contribution, with components as shown in Figure 5. Although limiters were initially fabricated on VPE layers, ion-implantation has been subsequently used with good results. The doping densities are 1.0E17 cm-3 for the active layer and 1.0E18 cm-3 for the contact layer. The resulting sheet resistance is about 100 ohms/square.

The fabrication process begins with mesa isolation for active device and resistor areas. AuGeNi ohmic contacts are subsequently deposited and alloyed at 460°C. Diode anode formation uses contact lithography for definition of the 0.8 µm and 1.5 µm anode fingers. TiPtAu metallization is deposited using a bi-level photoresist liftoff scheme. Anodes are recessed through the n+ layer using a FET test structure as a recess etch monitor. Capacitor bottom metallization is then defined via liftoff. Capacitor dielectric and diode passivation are formed by plasma enhanced chemical vapor deposition of silicon nitride to 1500 Angstrom thickness. Each wafer is dc autotested for twenty different electrical parameters before die separation by diamond scribing.

Limiter Operation

Limiter power transfer characteristics and typical second harmonic levels are shown in Figure 6. The relatively low (~40 dBc) second harmonics are a result of the limiter symmetry and the near identity of diode characteristics [5] - a situation enhanced by the GaAs MMIC realization. Limiter output power range for various levels of compression and bridge dc bias are shown in Figure 7. Limiting threshold (0.5 dB compression) is adjustable over a 6 dB range.

The incorporation of r_{SH} (Figure 3) assures low input VSWR (typically 2.0:1) for the full input dynamic range. This beneficial effect of incorporating r_{SH} is traded off vs. compression threshold and "hardness" of limiting, as demonstrated in Figures 7 a) and b) (input and output are reversed). Clearly, limiting characteristics would be improved if $r_{SH} = 0$ (at the expense of input VSWR). This is the preferred configuration for certain applications.

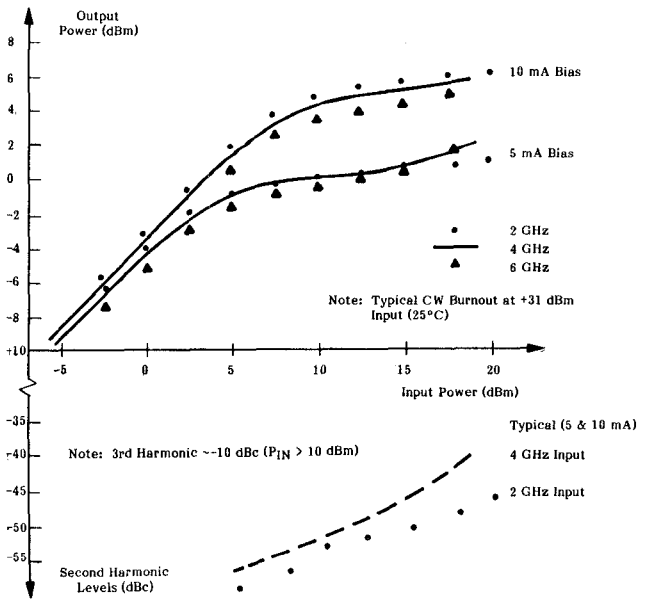

Figure 6. Measured Limiter Power Transfer and Typical Second Harmonic Characteristics

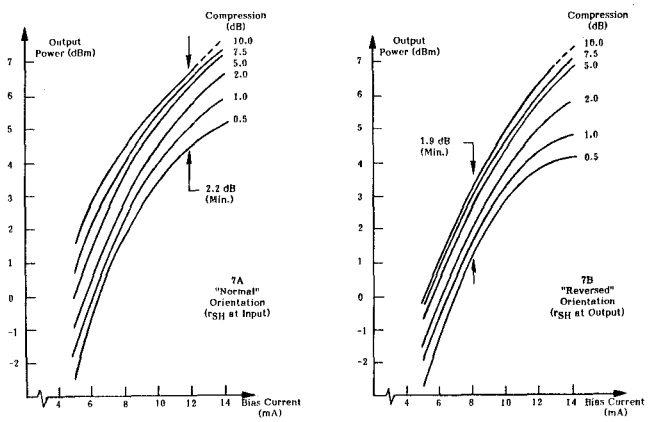

Figure 7. Limiter Compression as a Function of DC Bias

Three Stage Limiting Amplifier

The GaAs FET gain stage developed for this application (Figure 8) is a conventional (quadrature hybrid) balanced design for which the output circuitry was designed for nearly optimum power match using the techniques reported by Cripps [6]. The devices employed are WJF105R recessed gate 0.5 µm x 300 µm GaAs FETs. Typical performance over a 2 - 6 GHz bandwidth is: Gain, 13.0 dB; $P_{1\ dB}$, 19 dBm; P_{SAT}, 21 dBm; second harmonic intercept point, +47 dBm; noise figure, 4.7 dB.

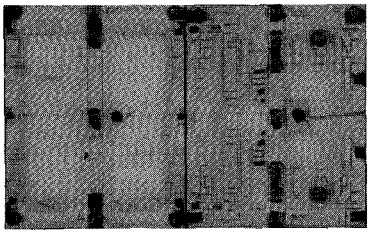

Figure 8. Balanced Limiter and Balanced GaAs FET Amplifier Pair

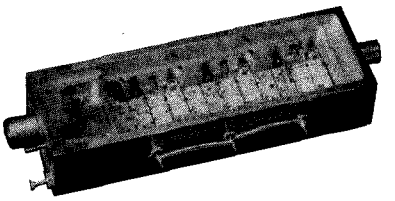

Figure 9. Three Stage Limiting Amplifier Prototype Utilizing Limiter/Amplifier Pairs

Two limiter ICs were incorporated in a (quadrature hybrid) balanced circuit module. This "balanced" configuration offers virtually no improvement in second harmonic rejection, but does provide a degree of third harmonic cancellation (20 dB typical - a consideration for bandwidths exceeding 3:1) and improved VSWR. The three stage limiting amplifier consisting of hybrid circuit modules (3 limiters/3 gain stages) is shown in Figure 9. Small signal gain was 27.0 ± 1.5 dB over a 2 - 6 GHz bandwidth. Typical power transfer and second harmonic response is shown in Figure 10.

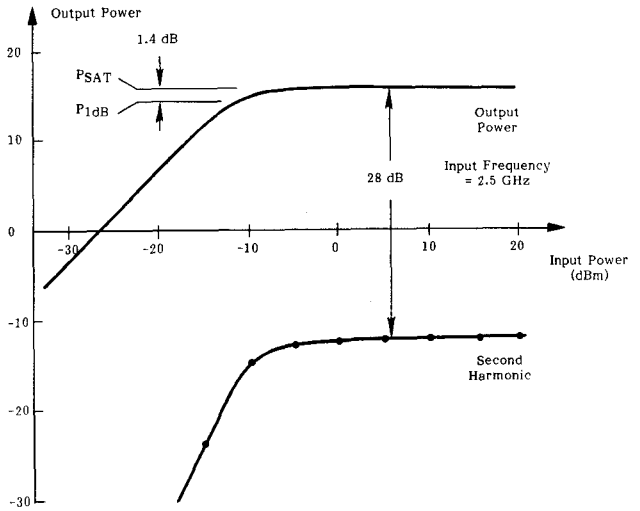

Figure 10. Three Stage Limiting Amplifier Power Transfer and Harmonic Characteristics

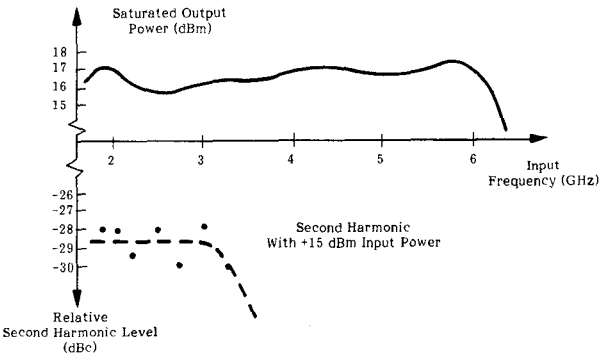

Figure 11. Three Stage Limiting Amplifier Saturated Output Power and Second Harmonic Levels vs. Frequency

The limiting function compresses a 31 dB input dynamic range (-11 dBm to +20 dBm) into a 1.4 dB output range ($P_{1\ dB}$ to P_{SAT}) at a typical single frequency. As shown in Figure 11, saturated output power over 1.7 to 6.0 GHz was 16.6 ± 0.8 dBm, and second harmonics were suppressed by a minimum of 28 dB - substantially more than previously reported for amplifiers of similar operating bandwidth.

Pulsed response measurements for an input level of +15 dBm (causing amplifier saturation) have demonstrated rise and fall times of less than 3.0 nanoseconds, apparently limited by the pulse modulation test apparatus available. The ability to transition rapidly from saturated to linear operation is due to the limiters functioning to maintain the amplifier stages in a linear operating region for all signal conditions.

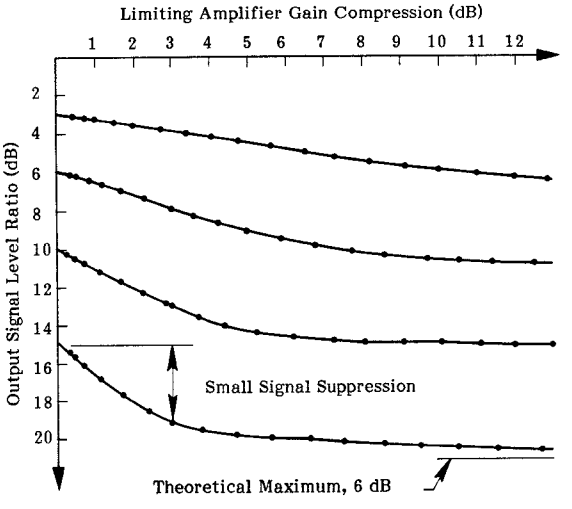

Figure 12. Relative Output Levels of Two Simultaneous Signals as a Function of Limiting Amplifier Gain Compression (Measured Data, F_1 = 2.9 GHz, F_2 = 3.0 GHz)

Two-tone small signal suppression measurements were performed, with typical results presented in Figure 12. The difference between the two output signals (3, 6, 10, 15 dB) was set for small signal operating conditions. Then the two signals were increased by equal amounts, and the gain compression and output signal ratios were measured using power meters and a spectrum analyzer. The amount of increased signal separation (suppression) was observed to be a function of both the amount of limiting (gain compression) and input signal separation. For large input signal separation (15 dB), small signal suppression occurs rapidly with the onset of limiting and equals 5 dB at 6 dB compression. Small signal suppression occurs much more gradually (requires more compression) and is significantly less for smaller input signal separation. These results are in good agreement with Jones' theory [7] for an ideal limiter, in which the maximum small suppression is shown to be 6.0 dB for large input signal separation, and 4.0 dB for an input power ratio of 3.0 dB. The data of Figure 12 also provides insight as to the difficulty in achieving ideal suppression characteristics for broadband multistage limiting amplifiers, particularly for signals of nearly equal amplitude and large separation in frequency. Small deviations from (ideally) constant gain (as a function of frequency) of the individual amplifier stages affect the relative signal levels present at the limiters, and thus the composite suppression characteristics.

Conclusions

A broadband limiting amplifier design consisting of MMIC limiters alternating with GaAs FET amplifier stages has been presented. The MMIC limiter incorporates GaAs Schottky diodes in a shunt-series bridge-shunt configuration, which strongly suppresses even harmonic generation due to circuit symmetry. The function of the limiters in the overall limiting amplifier is to restrict signal levels such that the GaAs FET gain stages operate in a linear region. A three stage prototype limiting amplifier maintained second harmonic levels at least 28 dB below the fundamental output, when driven 30 dB into saturation. Pulse response time is less than three nanoseconds, and small signal suppression measurements were in close agreement with established theory. This limiting amplifier design can be expected to find application in a variety of systems requiring limiting with low harmonic distortion, including instantaneous frequency measurement (IFM) receivers, channelized receivers, and frequency memory loops (FMLs).

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